## CLAIMS:

What is claimed is:

1. A set of at least one component to handle packets, comprising:

a first component, comprising:

an input interface to receive data of packets;

an output interface;

circuitry to:

generate packets including a header and a payload such that data values within the generated packet payloads include data originating within the first component; and

transmit packets via the output interface to a component further along a receive path monotonically ascending layers of a protocol stack, the packets to transmit including the generated packets and packets including data of packets received via the input interface.

2. The set of at least one component to handle packets of claim 1,

wherein the first component comprises a PHY.

3. The set of at least one component to handle packets of claim 2,

wherein the input interface comprises signal to digital conversion circuitry,

the circuitry operating on at least one of the following: optic signals, wire signals, and wireless signals.

4. The set of at least one component to handle packets of claim 2,

wherein the output interface comprises a Media Independent Interface .

5. The set of at least one component to handle packets of claim 2,

wherein the data originating within the first component comprises at least one status of the PHY.

6. The set of at least one component to handle packets of claim 5,

wherein the at least one status comprises at least one of: link up and link down.

7. The set of at least one component to handle packets of claim 5, wherein the data originating within the first component further comprises at least one of a sequence number and a timestamp.

8. The set of at least one component to handle packets of claim 2,

wherein the PHY further comprises circuitry to determine when to transmit the generated packets.

9. The set of at least one component to handle packets of claim 2,

further comprising a second component, the second component to identify packets generated by the PHY.

10. The set of at least one component to handle packets of claim 9, wherein the second component comprises a component to intercept the packets generated by the PHY.

11. The set of at least one component to handle packets of claim 9,

wherein the second component comprises at least one of a framer, a device driver, and a processor.

12. The set of at least one component to handle packet of claim 2, wherein the PHY further comprises circuitry to intercept PHY configuration packets traveling along a transmit path monotonically descending the layers of the protocol stack.

13. The set of at least one component to handle packets of claim 1,

wherein the first component comprises a framer.

14. The set of at least one component to handle packets of claim 13,

wherein the input interface comprises an interface to a PHY.

15. The set of at least one component to handle packets of claim 13,

wherein the output interface comprises a System Packet Interface (SPI).

16. The set of at least one component to handle packets of claim 13,

wherein the data originating within the framer comprises at least one network interface statistic.

17. The set of at least one component to handle packets of claim 16,

wherein the at least one network interface statistic comprises at least one of: packets received, packets transmitted, bytes received, and bytes transmitted.

18. The set of at least one component to handle packets of claim 16, wherein the data originating within the framer further comprises at least one of a sequence number and a timestamp.

19. The set of at least one component to handle packets of claim 13,

wherein the framer further comprises circuitry to determine when to transmit the generated packets.

20. The set of at least one component to handle packets of claim 13,

further comprising a second component, the second component to identify packets generated by the framer.

21. The set of at least one component to handle packets of claim 20, wherein the second component comprises a component to intercept the packets generated by the PHY.

22. The set of at least one component to handle packets of claim 13,

wherein the framer comprises at least one of: an Ethernet media access controller (MAC), a High-Level Data Link (HDLC) framer, and a Synchronous Optical NETwork (SONET) framer.

23. The set of at least one component to handle packets of claim 13, wherein the framer further comprises:

a second input interface to receive packets along a transmit path;

a second output interface; and

circuitry to:

identify packets in the transmit path destined for the framer;

examine the contents of a packet destined for the framer, the contents identifying at least one of: at least one statistic to include in the generated packets, a request to generate at least one packet, at least one time to generate at least one of the generated packets; and

transmit packets not destined for the framer via the second output interface to a component further along a transmit path monotonically descending layers of a protocol stack.

24. The set of at least one component to handle packets of claim 1, wherein the first component comprises a component to:

configure packet generation based on configuration packets received by the first component; and

eliminate the configuration packets from their packet stream.

25. The set of at least one component to handle packets of claim 1,

wherein the circuitry to generate packets comprises circuitry to generate a packet header identifying generated packets to a component further along the receive path.

26. The set of at least one component to handle packets of claim 1,

wherein the set of at least one component comprises a PHY component and a framer component, and

wherein at least one of the PHY component and the framer component comprises the circuitry to generate packets in the receive path.

27. The set of at least one component to handle packets of claim 1, wherein the set comprises at least one component of a network interface controller (NIC).

28. A method, the method comprising:

generating, at a first component, a packet having a header and payload, the payload including data originating within the first component; and

transmitting the packet to a second component further along a receive path monotonically ascending layers of a protocol stack.